



# MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE

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## A Report on


### IEEE CASS SEASONAL SCHOOL TITLED "NEUROMORPHIC COMPUTING AND LOGIC IN MEMORY COMPUTING USING NON-VOLATILE MEMORY DEVICES"

Organized by

Department of Electrical & Electronics Engineering (EEE) in association with IEEE Student Chapter, MITS Madanapalle

23/09/2024 to

25/09/2024

<p><b>About the Institute</b></p> <p>Madanapalle Institute of Technology &amp; Science (UGC-Autonomous Institution) popularly known as MITS, was established in 1998 in the picturesque and pleasant environment of Madanapalle and is ideally located on a sprawling 26.17 acre campus on Madanapalle - Ananthapuramu Highway (NH-205) near Angali, about 10 km away from Madanapalle and 120 km from Bangalore Airport. MITS was originated under the auspices of Ratakonda Ranga Reddy Educational Academy under the proactive leadership of Dr. N. Vijaya Bhaskar Choudary, Ph.D., Secretary &amp; Correspondent. It offers 11 Under Graduate Engineering Programmes, and 2 Post-Graduate Programmes (MBA and MCA). It has benchmarked its curriculum and teaching methodologies with premier Indian institutes to maintain academic excellence. It is a NAAC 'A+' accredited institution and all the eligible programmes have been accredited by NBA. MITS is ranked among the 251-300 band of NIRF - 2022 Ranking. MITS has entered into MoUs with 17 renowned universities across the world. 52 B.Tech students got selected for University Innovation Fellowship program (UIF) of Stanford University, USA and many students have completed their internships in Taiwan, Japan, Germany, Finland, Russia, Dubai and Singapore. The Institute has around 6,500 students, 363 Teaching Faculty, among which 188 Faculty members are with Ph.D qualification from many renowned Indian and foreign Universities. In addition to these resources, the latest inclusion is MITS - Community Radio 90.8 which is established to foster students' involvement and participation to provide the most recent updates of Science and Technological advancements to the community.</p>	<p><b>Organizing Committee</b></p> <p>Chief Patron Dr. N. Vijaya Bhaskar Choudary Secretary &amp; Correspondent</p> <p>Patron Mrs. Keerthi Nadella Executive Director</p> <p>Programme Chair Dr. C. Yuvaraj Principal</p> <p>Convener Dr. Nehru Kandasamy Professor</p> <p><b>Advisory &amp; Organizing Committee Members</b></p> <p>Dr.C.Kamal Basha,VP-Administration Dr.P.Ramanathan,VP-Academics Dr.R.Thulasiram Naidu,R&amp;D Advisor Dr.P.Sivaiah, R&amp;D Associate Dean Dr. A.V. Pavan Kumar, EEE HOD Dr. C. Kumar, IEEE Coordinator</p>	 <p><b>MADANAPALLE INSTITUTE OF TECHNOLOGY &amp; SCIENCE</b> (UGC-AUTONOMOUS INSTITUTION) Madanapalle-517325, Annamaya Dist., Andhra Pradesh</p> <p><b>IEEE CAS SEASONAL SCHOOL ON "NEUROMORPHIC COMPUTING AND LOGIC IN MEMORY COMPUTING USING NON-VOLATILE MEMORY DEVICES"</b></p> <p>SPONSORED BY <b>IEEE CIRCUITS AND SYSTEMS SOCIETY</b></p> <p>SUPPORTED BY <b>IEEE HYDERABAD SECTION</b></p>
<p><b>About the Seasonal School</b></p> <p>School Title: Seasonal School on "Neuromorphic Computing and Logic In Memory Computing Using Non Volatile Memory Devices"</p> <p><b>Description of the seasonal School</b></p> <p>This seasonal school covers variety of topics related to fundamentals, ongoing research and future trends related to Non-Volatile Memories for logic In Memory computing as well as Neuromorphic Computing Applications. Experts from National University of Singapore, Nanyang Technological University, Singapore, Fraunhofer IPMS - Germany, CNRS France, University of Tennessee-United Kingdom, University of Sheffield-United Kingdom, Queen's University, Canada, University of Edinburgh- United Kingdom, IBM Research Zurich, Switzerland and Indian Institute of Technology Kanpur - India.</p>	<p><b>Registration Details</b></p> <p>Registration Fees (for Students, Researchers, and Faculty Members), Including the Discount for CAS Society Members:</p> <ul style="list-style-type: none"> <li>Rs.400 for IEEE CAS Members.</li> <li>Rs.500 for IEEE Members.</li> <li>Rs.600 for Non-IEEE Members.</li> </ul> <p>Last Date for Registration : 20/09/2024</p>	
<p><b>Contact Details</b></p> <p>Dr. Nehru Kandasamy Professor, Electronics and Communication Engineering Madanapalle Institute of Technology and Science IEEE Senior Member Research Fellow, National University of Singapore (2019-2022) Email : drnehruk@mits.ac.in Contact : +91 9940529189</p>	<p><b>Registration and payment Link</b></p> <p><a href="https://forms.gle/ZDkS1EBuvFxd9Fq6">https://forms.gle/ZDkS1EBuvFxd9Fq6</a></p> <p>Seasonal School Website: <a href="http://www.mits.ac.in/sscas">www.mits.ac.in/sscas</a></p>	 <p><b>SEASONAL SCHOOL 2024</b> 23-25 SEPTEMBER 2024 <a href="http://www.mits.ac.in">www.mits.ac.in</a></p>

**Chief Convener: Dr. AV Pavan Kumar, Professor and Head, Department of EEE, MITS.**

**Convener: Dr. Nehru Kandasamy, Professor, ECE**

**Resource Person/Speaker: Details attached below**

**Attendees: 71 members (National and International)**

**Venue: Seminar Hall**

**Time: 10:00 AM**

## Resource Person/ Speaker:

S.no	Eminent keynote Speaker details	University
1	Dr Kim Tae Hyoung	Associate Professor, School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore
2	Dr FONG, Xuanyao Kelvin	Assistant Professor, Electrical and Computer Engineering, National University of Singapore, Singapore
3	Dr. Thomas Kämpfe	Group Manager Integrated RF & AI Fraunhofer IPMS (Center Nanoelectronic Technologies CNT) An der Bartlake 5, 01109 Dresden, Germany
4	Dr Damien QUERLIOZ	<b>Research Director, CNRS</b> Adjunct Professor, Université Paris-Saclay Centre de Nanosciences et de Nanotechnologies 10 Boulevard Thomas Gobert, 91120 Palaiseau, France
5	Dr. Catherine Schuman	Assistant Professor, Department of Electrical Engineering and Computer Science University of Tennessee, United Kingdom
6	Dr. Merlyne De Souza	Professor, Department of Electronic and Electrical Engineering University of Sheffield, United Kingdom
7	Dr. Shubham Sahay	Assistant Professor, Department of Electrical Engineering Indian Institute of technology Kanpur India
8	Dr Sakthivel R	Professor, School of SENSE, VIT university, Vellore
9	Dr. Shady Agwa	Research Fellow, Centre for Electronics Frontiers CEF, University of Edinburgh, United Kingdom
10	Dr. Laura Bégon-Lours	Assistant Professor @ETH Zurich, Researcher in Material for AI Hardware Zurich

Participants: 71 members from National and International

Venue: Seminar Hall A, Madanapalle Institute of Technology and Science

Time Schedule in Indian Standard Time:

1. Dr FONG, Xuanyao Kelvin, Assistant Professor, Electrical and Computer Engineering, National University of Singapore, Singapore.  
Date: 23/9/2024, Meeting Time: 11 AM – 12.30 AM IST
2. Dr Kim Tae Hyoung, Associate Professor, School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore.  
Date: 23/9/2024, Meeting Time : 2 PM – 3.30 PM IST

3. Dr Damien QUERLIOZ      Research Director, CNRS Adjunct Professor, Université Paris-Saclay Centre de Nanosciences et de Nanotechnologies 10 Boulevard Thomas Gobert, 91120 Palaiseau, France  
Date: 23/9/2024, Meeting Time: 4 PM – 5 PM IST
4. Dr. Shubham Sahay    Assistant Professor, Department of Electrical Engineering Indian Institute of technology Kanpur India  
Date: 24/9/2024, Meeting Time: 10 AM – 11.30 AM IST
5. Dr. Merlyne De Souza, Professor, Department of Electronic and Electrical Engineering, University of Sheffield, United Kingdom  
Date : 24/9/2024 , Meeting Time : 2 PM – 3 PM IST
6. Dr. Thomas Kämpfe, Group Manager Integrated RF & AI, Fraunhofer IPMS (Center Nanoelectronic Technologies CNT) An der Bartlake 5, 01109 Dresden,Germany  
Date : 24/9/2024, Meeting Time: 3.30 PM – 4.30 PM
7. Dr . Sakthivel Ramachandran, Professor, School of Electronics, Vellore Institute of Technology  
Date : 25/9/2024, Meeting Time: 10.30 AM– 11.30 AM IST
8. Dr. Catherine Schuman,Assistant Professor, Department of Electrical Engineering and Computer Science University of Tennessee, United Kingdom  
Date : 25/9/2024, Meeting Time : 1.30 PM- 2.30 PM IST
9. Dr. Shady Agwa,Research Fellow, Centre for Electronics Frontiers CEF, University of Edinburgh, United Kingdom  
Date : 25/9/2024 Meeting Time: 3 PM – 4 PM IST
10. Dr. Laura Bégon-Lours, Assistant Professor, ETH Zurich  
Date: 25/9/2024 , Meeting Time: 5.30 PM to 6.30 PM

EMINENT SPEAKERS		Topics to be covered
 Dr Kim Tae Hyoung Nanyang Technological University Singapore	 Dr. Shubham Sahay Indian Institute of Technology Kanpur India	<ul style="list-style-type: none"> <li>• RRAM Based Logic in Memory Computing</li> <li>• STT MRAM based Logic in Memory Computing</li> <li>• FEFET based in Memory Computing</li> <li>• Neuromorphic computing with nanoscale spintronic oscillators</li> <li>• Energy Efficient Neromorphic Devices, Circuits and Systems based on 3D- NAND Flash</li> <li>• Spike Based Neuromorphic Computing for Next Generation Computer Vision</li> <li>• Neuristor for Advanced Neuromorphic Intelligent Systems</li> <li>• Neuromorphic Photonics</li> <li>• Digital In-Memory Stochastic Computing</li> <li>• Architecture for Vector-Matrix Multiplication</li> <li>• Neuromorphic Computing using Ferroelectric Based Devices</li> </ul>
 Dr FONG, Xuanyao Kelvin National University of Singapore Singapore	 Dr Bhavin Shastri Queen's University Canada	
 Dr. Thomas Kämpfe Group Manager Integrated RF & AI Fraunhofer IPMS, Germany	 Dr. Shady Agwa University of Edinburgh United Kingdom	
 Dr Damien QUERLIOZ CNRS France	 Dr. Laura Bégon-Lours IBM Research Zurich, ESPCI-PSL engineer Switzerland	
 Dr. Catherine Schuman University of Tennessee United Kingdom	<p><b>MADANAPALLE INSTITUTE OF TECHNOLOGY &amp; SCIENCE</b> (UGC-AUTONOMOUS INSTITUTION) Madanapalle-517326, Annamayya Dist., Andhra Pradesh <a href="http://www.mits.ac.in">www.mits.ac.in</a></p> 	
 Dr. Merlyne De Souza University of Sheffield United Kingdom		
<p>SPONSORED BY IEEE CIRCUITS AND SYSTEMS SOCIETY SUPPORTED BY IEEE HYDERABAD SECTION</p>    		

IEEE CASS Seasonal School Lecture Video Recorded Link :

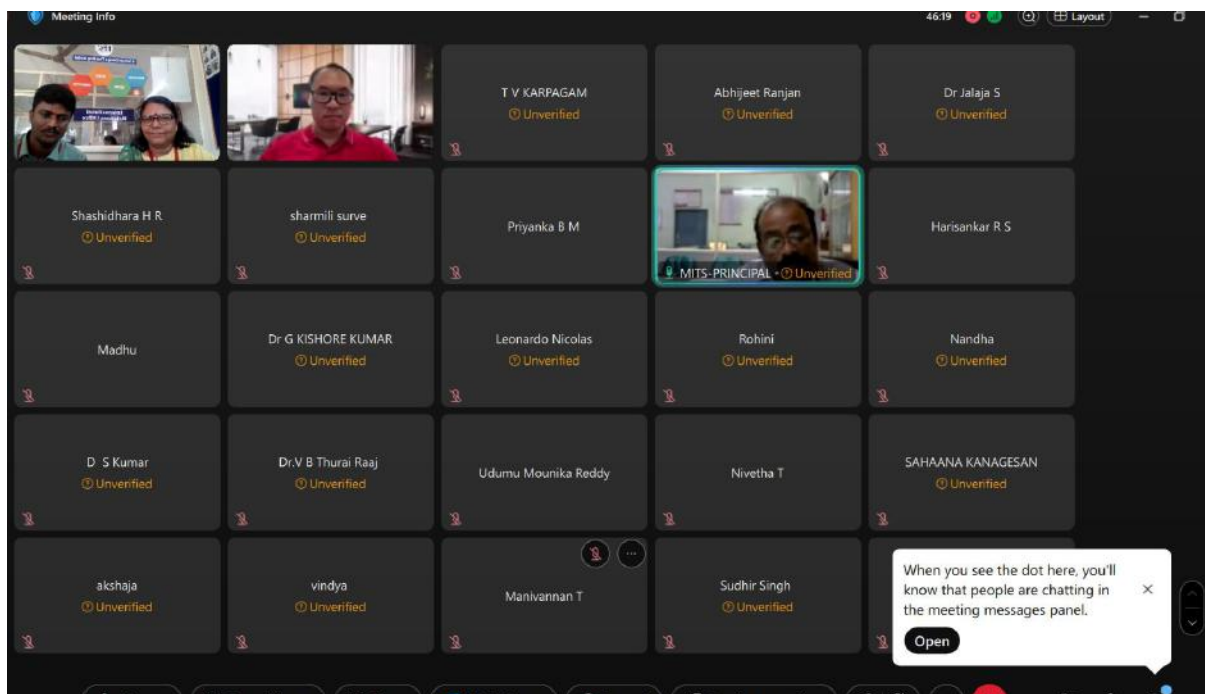


## Background :

The session was attended by Undergraduate students, Graduate students, Research scholars, Industry Persons and faculty members from the IEEE members, non IEEE members, Electronics department, Nanotechnology department and Semiconductor industry peoples, providing deep understanding of the technological advancements shaping the neuromorphic computing and logic in memory computing.

## Detailed Summary of the Event

The seasonal school began with warm welcome address delivered by Dr. Nehru Kandasamy, Professor, ECE and Special address by Dr.C.Yuvaraj, Principal , Madanapalle Institute of Technology and Science. Mrs. Vijayalakshmi ,Assistant Professor, International relationship manager introduced the chief guest Dr. Kelvin Fong , NUS to the participants .



## Session 1:

**Date & Time :** 23/9/2024, 11.00 AM – 12.00 PM IST

**Topic:** Logic In Spintronic Memories

Dr. FONG, Xuanyao Kelvin, Assistant Professor, Electrical and Computer Engineering, National University of Singapore, Singapore. He was delivered the keynote address with brief background of the spintronic memories.

- Spintronic Synapses
- Spintronic Based True Random Number Generator

IEEE CAS Seasonal School Meeting Info 02:10:41 Meeting Info

Dr. Kumar C Nehru Kandasamy Srija Unverified karpagam Unverified

Viewing Kelvin Fong (NUS)'s shared content 100%

### Spintronic Synapses

Domain wall and skyrmions synapses demonstrate excellent potential as linear synapses!

A. Sinigaglia et al., IEEE CAS 19(6), PRA 6(6400); W. Zhao et al., Nanotechnology 28(8),702; K. M. Soun et al., Nature Electronics 3, D. Das et al., PRApplied 19(10),400

Chat

Everyone Direct

Messages to everyone will be saved after the meeting.

spintronics ( spin wave) And it is different can you please explain summary Thanks

akshaja Unverified 12:29 PM  
what is primary source of entropy in spintronic based TRNG and how does it compare to conventional TRNGs in terms of randomness quality?

Srija Unverified 12:30 PM  
Hello Sir, from where can we obtain the open source verilog model files for different MTJ switching mechanisms??

Write a message to IEEE CAS

## Session 2

**Date & Time : 23/9/2024 , 2.00 PM – 3.30 PM IST**

**Topic: ReRAM based Compute In Memory**

Dr Kim Tae Hyung, Associate Professor, School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore.

Prof Kim Tae Hyung addressed the following points

- Machinelearning for edge devices
- ReRAM for Vector Matrix Multiplication
- ReRAM – Emerging NVM Technology

IEEE CAS Seasonal School Meeting Info 04:47:25 Layout

Dr. Kumar C akshaja Unverified Mrs. U. Vijaya Lakshmi Unverified Tony Kim Unverified

Viewing Tony Kim's screen 100% Annotate

### Logic-in-Memory Operation

- Turn on WLL/WLR in two rows simultaneously.
- Compare BL/BLB voltages with Vref.
- BL and BLB compute **AND(A, B)** and **NOR(A, B)**, respectively.
- Two SA outputs are NORed to perform **XOR(A, B)**.

[Chen et al., ISCAS 2020] 47 of 57

Chat

Everyone Direct

Messages to everyone will be saved after the meeting.

I do not understand how the MAC values overlap happen 8 bits and above?

VINDHYA Unverified 03:06 PM  
Does I-HRS affect the performance of the device?  
speed and accuracy both

Nehru Kandasamy 03:07 PM  
How to choose the vref value in sense amplifier for larger array size?

Write a message to IEEE CAS

Unmute Start video

Participants (35)

Invite and remind

Participants (35)

- Dr. Kumar C
- akshaja Unverified
- John Unverified
- Sahaana Kanagesan
- Priyanka B M
- Dr. Kumar C Host, me • ieee.org
- Tony Kim Presenter • Unverified
- Mrs. U. Vijaya Lakshmi Cohost • Unverified
- Nehru Kandasamy Cohost • ieee.org
- Venu C Cohost • ieee.org
- Adiba Unverified
- akshaja Unverified
- Ambole Yash Unverified
- D S Kumar Unverified
- DORATHY Unverified
- Dr Jalaja S

Mute all Unmute all More options

### Session 3

Date & Time : 23/9/2024 4.00 PM – 5.00 PM IST

Topic: Toward Energy Efficient and Trustworthy Embedded AI: The In Memory Computing Approach

Dr Damien Quarlioz, CNRS, France summarized his talk with the following points.

- Toward Energy Efficient and Trustworthy Embedded AI
- Multiplication within the sense amplifier
- Analog In Memory Computing

IEEE CAS Seasonal School Meeting Info 06:10:07 Layout

Viewing Damien Querlioz's shared content 110% +

## Analog In-Memory Computing Performs Neural Network Inference Very Naturally

A matrix of analog memristors naturally implements a layer of neural network with **Ohm's and Kirchhoff's laws!**

Memristor conductance  $G = \text{synaptic weight } w$

$$I_1 = t_1 = \sum w_{ij} s_i$$

Neuron value  $t_j = f(\sum w_{ij} s_i)$

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Dr. Kumar C

Mrs. U. Vijaya Lakshmi Unverified

Damien Querlioz Unverified

IEEE CAS Seasonal School Meeting Info 06:20:16 Layout

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## Memristor-Based Bayesian Neural Networks

We program 50 memristor-neural networks (each with two layers). We apply same input to them

**We get 50 outputs:** their dispersion tells about the *certainty* of the neural network

arrhythmia identification

Bonnet et al, Nature Communications 14, 7530 (2023)

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Dr. Kumar C

Mrs. U. Vijaya Lakshmi Unverified

Damien Querlioz Unverified

### Session 4

Date & Time : 24/9/2024 10.00 AM – 11.30 AM IST

Topic:Energy Efficient Neuromorphic Circuits and Systems based on 3D NAND Flash Memory

Dr. Shubham Sahay Assistant Professor, Department of Electrical Engineering, Indian Institute of technology Kanpur, India

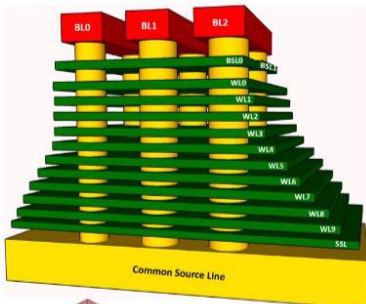
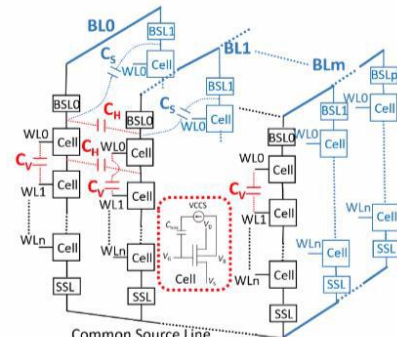
He was presented the following insightful key points in 3D NAND Flash

- 3D NAND Flash Compact Modelling Approach
- 3D NAND VMM Accelerator
- 3D NAND Inference Processor

karthikeyan Unverified akshaja Unverified John Unverified Dr. S... Unverified T V KARPAGAM Unverified

100%

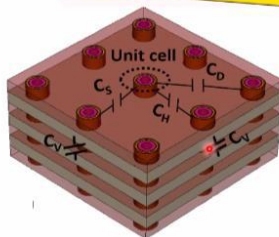
## Compact Modelling Approach

**3D-NAND Behavioral Compact Model**

Individual cells: GAANW (BSIM-CMG) with VCCS and BO capacitor

**Parasitic Capacitance extraction:**



S. Sahay and D. Strukov., A behavioral compact model for static characteristics of 3D NAND flash memory, *IEEE EDL*, vol. 40, 2019.

### Session 5

Date & Time : 24/9/2024 2.00 PM – 3.00 PM IST

Topic: Physical Reservoir Computing using a Solid Electrolyte TFT

Dr. Merlyne De Souza Professor, Department of Electronic and Electrical Engineering, University of Sheffield, United Kingdom

Prof Merlyne De Souza was delivered keynote related to reservoir computing using electrolyte TFT



IEEE CAS Seasonal School Meeting Info

Dr. Kumar C Priyanka B M akshaja John

Unverified Unverified Unverified Unverified

Viewing Dr. Shubham Sahay's screen 100% Annotate

## 3D-NAND VMM Accelerator

**3D-NAND VMM**

TDC=Time to Digital Conv.  
DTC=Digital to Time Conv.  
N=Neuron  
LS=Level Shifter  
DEC=Decoder

Single String

**Single String**

Allows usage of **COMMERCIAL** 3D-NAND flash for VMM without any modification

M. Bavandpour, S. Sahay et. al. "Mixed-Signal Vector-by-Matrix Multiplication Circuits based on 3D-NAND Memories for Neurocomputing, DATE 2020.

Dr. Kumar C Srista John Syed Manzoor Qasim Mrs. U. Vijaya Lakshmi

Unverified Unverified Unverified Unverified

erlyne's applications 100%

## From RNN to Reservoir Computing Networks

**Recurrent Neural Network (RNN)**

Input layer Hidden layer Output layer

**Reservoir Computing (RC)**

Input layer Reservoir 'Black Box' Readout layer

- Weight management of each Neuron results in very high complexity and expense of training.
- Network instability and less effective learning.
- Only the readout layer is trained resulting in significant cost reduction.

IEEE CAS Seasonal School Meeting Info 04:50:57 Layout

Dr. Kumar C Mrs. U. Vijaya Lakshmi Srija John

Viewing Merlyne's applications

### Implementation of a Physical Reservoir using the SEFET

- A reservoir (device) transforms temporal inputs into space-time dependent features.
- These features are used to train the readout function using Logistic Regression.
- 60,000 image samples from the MNIST database, and to test a separate 10,000 image sample set, not used in training. 7-fold cross-validation to avoid over fitting.

A. Gaurav, X. Song, S. Manhas, A. Gilra, E. Vasiliaki, P. Roy and M. M. De Souza, "Reservoir Computing for Temporal Data Classification Using a Dynamic Solid Electrolyte ZnO Thin Film Transistor," *Front. Electron.*, 2022.

Participants (29): Dr. Kumar C, Merlyne, Venu C, Adiba, akshaja, D S Kumar, Dr. Jalaja S, Harisankar R S, John, karthikeyan, kasturi

**Session 6**

Date & Time : 24/9/2024 , 3.30 PM – 4.30 PM

Topic : Ferro Electronics :From Memory to Neuromorphic Computing

Dr. Thomas Kämpfe Group Manager, Integrated RF & AI, Fraunhofer IPMS (Center Nanoelectronic Technologies CNT) An der Bartlake 5,01109 Dresden, Germany

Dr. Thomas Kampfe mainly address the different FEFET memory cell , Fefet based CAM and Fefet for Neuromorphic computing. He was discussed the following points

- Neuromorphic computing accelerators
- FEFET Technologies
- Compute in Memory Chip
- Ferroelectric Analog CAM

IEEE CAS Seasonal School Meeting Info 06:46:29 Layout

Viewing Thomas Kämpfe's screen

### Hyperdimensional Computing

#### Fefet MCAM cells – Associative Memory

1024-Dimensional FWH (µV/Bit) in this matrix mapped to the proposed architecture

Dr. Kumar C Thomas K. Mrs. U. Vijaya Lakshmi Nehru Kandasamy

Seite 31 24.09.2024 © Fraunhofer A. Kazemi, et al., lo-accuracy in-memory hyperdimensional computing with ferroelectric devices, Scientific Reports (under review)

Viewing Thomas Kämpfe's screen 100% + Annotate

### Ferroelectric Analog CAM

Comparing two inputs

Fixing one FeFET to HVT state, the 2FeFET CAM becomes an analog CAM, capable of doing a threshold detection.

Seite 27 24.09.2024 © Fraunhofer X. Yin, et al., Deep random forest with ferroelectric analog content addressable memory, Nature Electronics (under review)

## Session 7

Date & Time :25/9/2024, 10.30 AM– 11.30 AM IST

Topic:Neuron Modelling and Hardware Accelerator for AI and ML

Dr. Sakthivel Ramachandran, Professor, School of Electronics, Vellore Institute of Technology , Vellore

He was addressed about the following points

- Neural versus Digital Computing
- Multilayer Perceptrons
- Hebb's Learning Rule
- Training vs Inference

IEEE CAS Seasonal School Meeting Info 01:40:39 Layout

Viewing Dr.Sakthivel Ramachandran's shared content 100% +

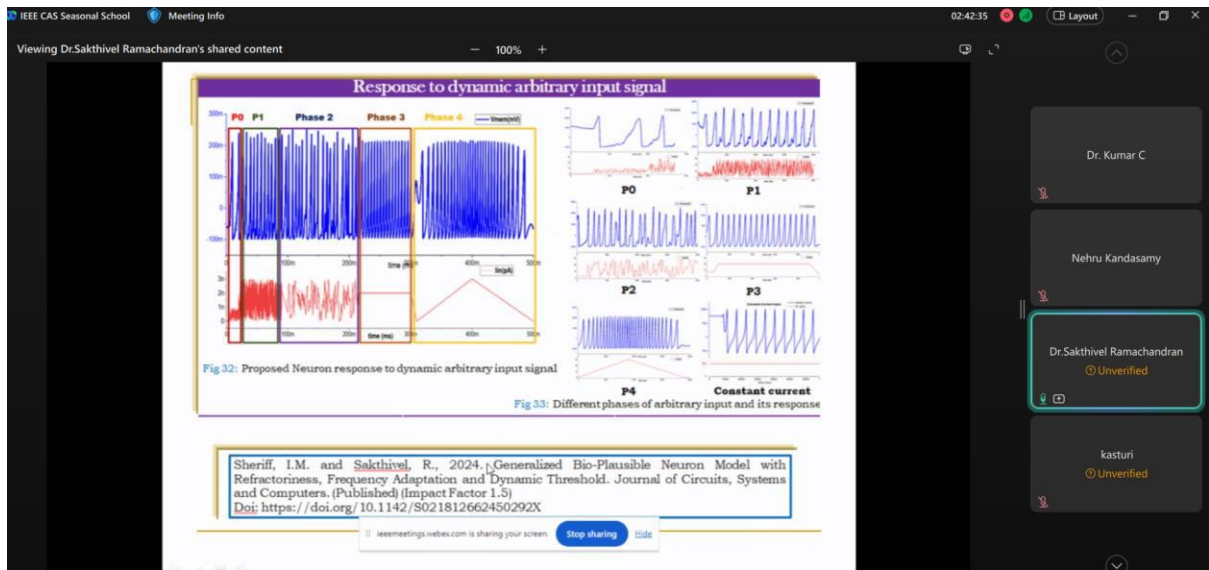
**Neuron Modelling and Hardware Accelerators for AI and ML**

Dr.R.SAKTHIVEL, Professor  
 Dept. Of Micro and Nano Electronics, VIT  
 Email: [rsakthivel@vit.ac.in](mailto:rsakthivel@vit.ac.in)  
 +91-9994627570

2024

Dr. Kumar C  
 Mrs. U. Vijaya Lakshmi Unverified  
 niharka Unverified

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## Session 8

Date & Time : 25-09-2024, 1.30 PM- 2.30 PM IST

Topic: Spike based Neuromorphic Computing for Next Generation Computer Vision

Dr. Catherine Schuman, Assistant Professor, Department of Electrical Engineering and Computer Science, University of Tennessee, United Kingdom

Prof Catherine Schuman has discussed about spiking neural networks, algorithm and Neuromorphic computing .

- Algorithm for Neuromorphic computing systems
- Spiking Neural Networks

### Neural Hardware and Neuromorphic Computing

#### Neural Hardware

Accelerates traditional neural network and deep learning computation

- Well-suited to existing algorithms
- Fast computation **or** low power
- Currently deployed in cloud or mobile devices

#### Neuromorphic Computing

Implements spiking recurrent neural network computation and can be suitable for neuroscience simulation

- Significant promise for future algorithmic development
- Fast computation **and** low power
- Still in development

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KNOXVILLE



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## TENNLab Neuromorphic Software Framework

Software Core: Common Interfaces, Input/Output Coding, Network Compiler

Architectures/Devices

mrDANNA DANNAZ RAVENS  
Our Hardware

Biom SOENS Caspian  
Collaborators' Hardware

External Simulators: Brian, NEST, BindsNET, Nengo, NengoLoihi

Plank, J. S., Schuman, C. D., Bruer, G., Dean, M. E., & Ross, G. S. (2016). The TENNLab exploratory neuromorphic computing framework. *IEEE Letters of the Computer Society*, 1(2), 17-20.

THE UNIVERSITY OF TENNESSEE KNOXVILLE

Chat

Everyone Direct

Messages to everyone will be saved after the meeting.

CAS - Host

Dr.Sakthivel Ramachandran Unverified 11:5  
rsakthivel@vt.ac.in  
9994627570

Dr.Sakthivel Ramachandran Unverified 11:5  
Dr.Sakthivel Ramachandran

New messages

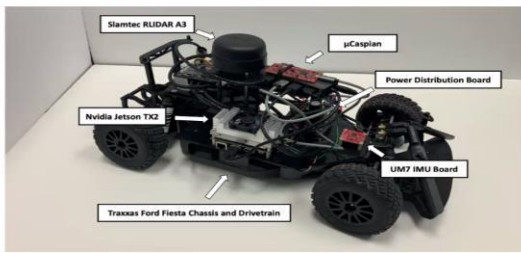
John Unverified 01:48 PM  
Could you explain a bit more on how the conventional backpropagation method is adapted for non-differentiability of SNN ?

Write a message to IEEE CAS

Viewing Katie Schuman's shared content

## F1Tenth: Autonomous Racing

- Fully autonomous 1/10th scale racing of Formula One (<https://f1tenth.org/>)
- Like full scale vehicles, the need for low size, weight, and power is critical
- Relatively inexpensive real-world demonstration of what neuromorphic computing can provide



THE UNIVERSITY OF TENNESSEE KNOXVILLE

Chat

Dr. Kumar C

Mrs. U. Vijaya Lakshmi Unverified

Katie Sch. Unverified

Nehru Kandasamy

## Session 9

**Date & Time : 25.09.2024, 3 PM – 4 PM IST**

**Topic: Digital In Memory Stochastic Computing Architectures**

Dr. Shady Agwa, Research Fellow, Centre for Electronics Frontiers CEF, University of Edinburgh, United Kingdom

He has enlightened the following points in his presentation.

- AI Vision
- Analog In Memory Computing
- Digital in Memory Computing
- In Memory Stochastic Computing

IEEE CAS Seasonal School Meeting Info 06:02:26

Viewing Shady Agwa's shared content 100%

## The AI Invasion!

3

IEEE CAS Seasonal School Meeting Info 06:18:16

Viewing Shady Agwa's shared content 100%

## Brain-Inspired Prescription!

- ✓ Gigantic Dense Memory
- ✓ Massive Parallel Processing
- ✓ Memory & Computation are Tightly Coupled
- ✓ Simple Data Representation (Spikes I\_III\_II\_III\_)
- ✓ Specialized & Approximate Computation
- ✓ High Resiliency

11

Dr. Kumar C

Shady Agwa (Unverified)

Nehru Kandasamy

John (Unverified)

IEEE CAS Seasonal School Meeting Info 06:31:23

Viewing Shady Agwa's shared content 100%

## Digital IMC!

SRAM - IDLE

SRAM - READ

SRAM - BLC

6T SRAM Bitcell

- Pre-Charge BL & BL<sub>o</sub>
- Activate WL
- Sense BL vs. BL<sub>o</sub>
- Data D is ready.

- Pre-Charge BL & BL<sub>o</sub>
- Activate Two WLs
- Sense BL & BL<sub>o</sub> vs. V<sub>REF</sub>!
- AND & NOR are ready.

© S. Jeloka, N. B. Akesh, D. Sylvester, and D. Blaauw. A Configurable TCAM/BCAM/SRAM Using 28nm Push-Rule 6T Bit Cell. Symp. On Very Large-Scale Integration Circuits (VLSIC), Jun 2015.

18

Dr. Kumar C

Shady Agwa (Unverified)

Nehru Kandasamy

John (Unverified)

IEEE CAS Seasonal School Meeting Info

Viewing Shady Agwa's shared content 100%

## In-Memory Stochastic Computing Architecture!

Projection using 4KB Modeling

Compared to 8-bit In-SRAM Computing (28nm)		
SC	16-bit	4-bit
Energy Efficiency	60x	250x
Throughput	10x	50x

© K. Al-Hawaj, et al., "Towards a Reconfigurable Bit-Serial/Bit-Parallel Vector Accelerator using In-Situ Processing in SRAM," IEEE ISCAS, pages 1-5, Oct 2020. 28

### Session 10

Date & Time : 25.09.2024, 05.30PM to 06.30PM (IST)

Topic: Ferroelectric Hafnia Superlattices for Bio Inspired Computing

Dr. Laura Bégon-Lours, Assistant Professor, ETH Zurich

She was addressed about CMOS integration of HZO, the novel  $\text{HfO}_2 / \text{ZrO}_2$  superlattice synaptic weights, the novel  $\text{HfO}_2 / \text{ZrO}_2$  superlattice FeCAPs, multi level 1T-1R and 1T-1C experimental works.

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### Ferroelectric tunnel junctions at IBM: $\text{HfZrO}_4/\text{WO}_x$ bilayers

- Atomic Layer Deposition of TiN /  $\text{HfZrO}_4$  /  $\text{WO}_x$  / TiN
- Crystallisation by millisecond Flash Lamp Annealing (E. O'Connor et al. (2018))
- Device definition by Reactive Ion Etching & Ion Beam Etching

Back-End-Of-Line integration:  
constraint on the thermal budget (<400C)

Neuromorphic chips design:  
constraint on the device footprint (<  $10\mu\text{m}^2$ ) +  
constraint on  $I_{\text{OFF}}$  &  $I_{\text{ON}}$

Laura Bégon-Lours / 25 September 2024 / ETH & IBM Research / IBM Research Zurich

Dr. Kumar C

Shady Agwa (Unverified)

Nehru Kandasamy

John (Unverified)

nilesh (Unverified)

Harisankar R S

Prof. Bégon-Lours (Unverified)

D Sai Kiran Reddy (Unverified)

#### Oxide Interfaces

Example of the Ferroelectric Tunnel Junction

HZO deposition: TiN, TiN, TiNO<sub>2</sub>, TiNO<sub>2</sub>

Snipping Tool

Screenshot copied to clipboard and saved

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### Research on novel materials: HfO<sub>2</sub> / ZrO<sub>2</sub> superlattices

**Fig. 1 Atomic-scale design of negative capacitance in ultrathin HfO<sub>2</sub>-ZrO<sub>2</sub>.**

Cheema et al. (2022): In HfO<sub>2</sub> / ZrO<sub>2</sub> / HfO<sub>2</sub> trilayer, ferroic order at the nanoscale and capacitance boost

**Fig. 1 Domain density as a function of the DE spacer thickness in FE/DEFE SL stack. Red and blue regions indicate domains within the FE which are pointing in opposite directions. Yellow region indicates the DE spacer region.**

Aabrar et al. (2022): In HfO<sub>2</sub> / HZO superlattices, decrease of the lateral domain size

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Participants (25)

Invite and remind

Dr. Kumar C

Nehru Kandasamy

Prof. Bégon-Lours Laura ETH Zurich

D Sai Kiran Reddy

John

aryan

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### Ferroelectric Hafnia Superlattices for Bio-Inspired Computing.

Laura Bégon-Lours<sup>\*1,2</sup>, Ruben Hamming-Green<sup>4,5</sup>, Mattia Halter<sup>1,2</sup>, Stefan Slesazek<sup>3</sup>, Elisabetta Morabito<sup>2</sup>, Donato Francesco Falcone<sup>2</sup>, Beatriz Noheda<sup>4,5</sup>, Bert Jan Offrein<sup>2</sup>

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- The authors acknowledge the Binnig and Rohrer Nanotechnology Center (BRNC)

ETH zürich IBM

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Prof. Bégon-Lours Laura ETH Zurich

Nehru Kandasamy

D Sai Kiran Reddy

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### Neuromorphic chips:

UNICO: ANR-19-CHR3-0006

**Voltage-Dependent Synaptic Plasticity (VDSP):**  
 Unsupervised probabilistic Hebbian plasticity rule based on neurons membrane potential  
 Nikhil Garg (CNRS, University of Sherbrooke)  
 DOI: 10.3389/fnins.2022.983950

BeFerroSynaptic: H2020-ICT-2019-2

**BEOL technology platform based on ferroelectric synaptic devices for advanced neuromorphic processors**  
 Institute of Neuroinformatics (UZH), NaMLab, University of Groningen  
<https://beferosynaptic.eu/publications>

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9

Participants (25)

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Prof. Bégon-Lours Laura ETH Zurich

Nehru Kandasamy

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Group Photo :



Sample Participant Certificate :



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The IEEE CASS seasonal school was concluded with vote of thanks to participants , circuits and systems society chair and resource persons by Dr. C. Kumar , Assistant Professor, Madapalle Institute of Technology and Science.

**Course Outcomes :**

At the end of the IEEE CASS Seasonal School all the Participants are able to understand the

- Basics of Neuromorphic Computing & Logic In Memory Computing
- Algorithm , device physics and Hardware/software integration of novel non volatile memory devices
- Real time applications using Non Volatile memory devices

Report Submitted by:

A handwritten signature in black ink that reads "Vineet Kumar". The signature is written in a cursive style and is underlined with a single horizontal stroke.

Dr. Vineet Kumar,  
Assistant Professor, EEE.